

Diagram illustrating a cross-sectional view of a semiconductor device. The device includes a substrate 11 with a layer 320. A gate structure GD1 is positioned on the left, and a gate structure GD2 is positioned on the right. A contact structure AP is located on the right side. A dashed line HL indicates a horizontal level, and a dashed line HD indicates a diagonal level.



FIG. 18
(PRIOR ART)

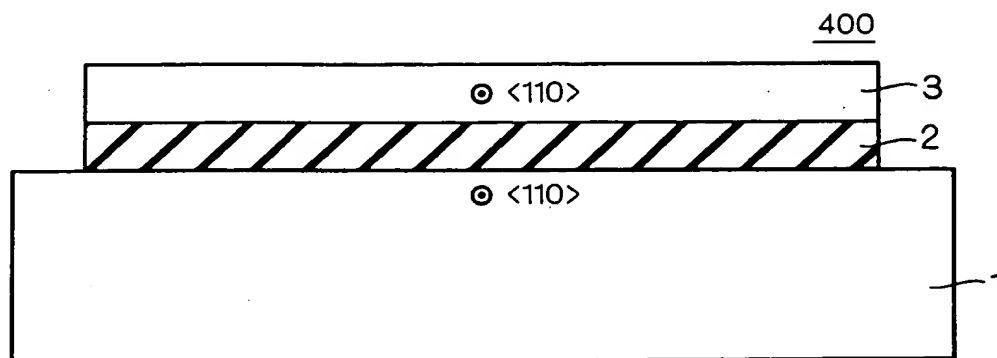


FIG. 19
(PRIOR ART)

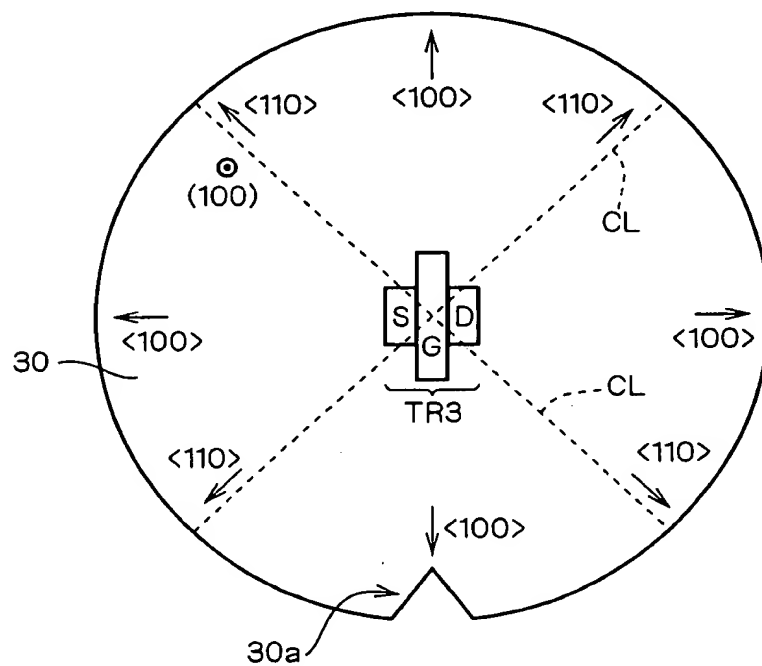




FIG. 20
(PRIOR ART)

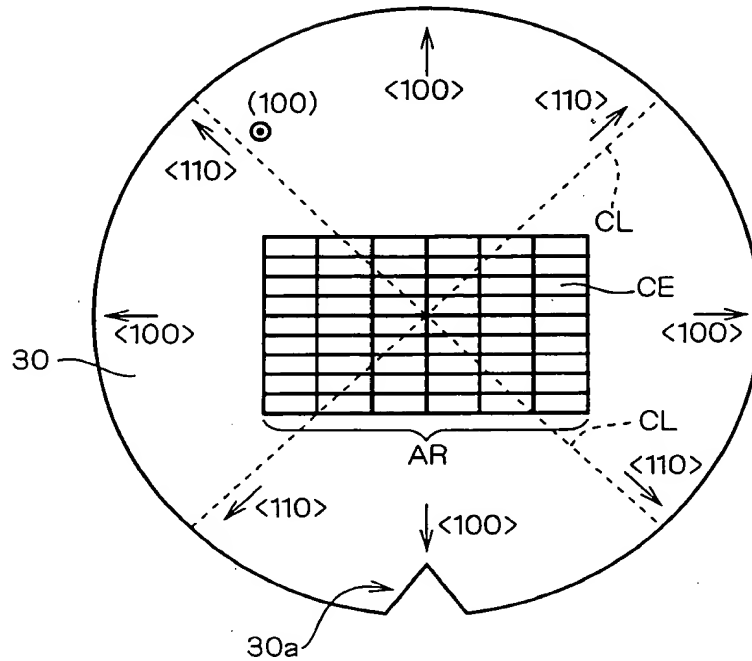


FIG. 21
(PRIOR ART)

